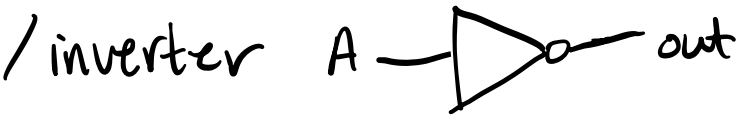
PHYS 231 - Nov. 8, 2023

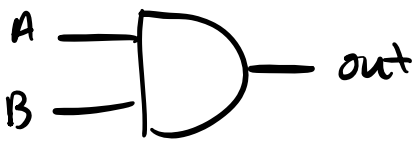
Logic Gates:

NOT / inverter



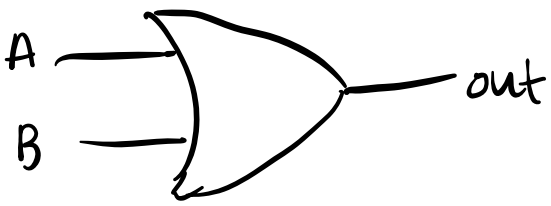
A	out = $\bar{A}$
0	1
1	0

AND



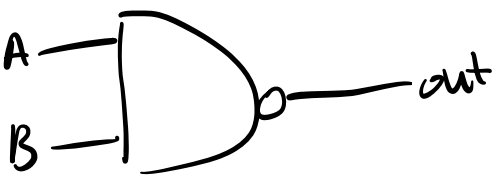
A	B	out = A·B
0	0	0
0	1	0
1	0	0
1	1	1

OR



A	B	out = A+B
0	0	0
0	1	1
1	0	1
1	1	1

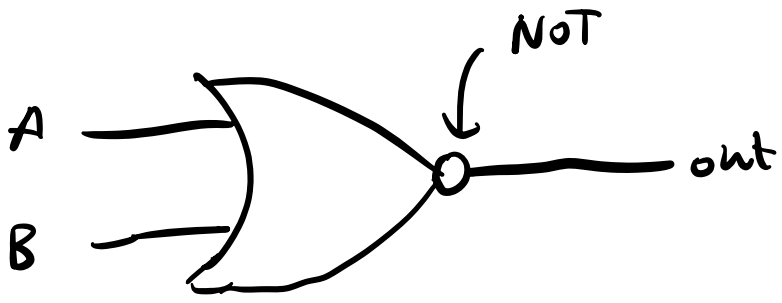
NAND



A	B	out = $\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

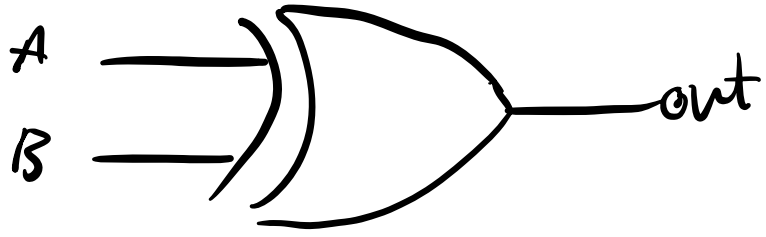
Other Logic gates

NOR (NOT OR)



A	B	out = $\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

XOR (Exclusive OR)

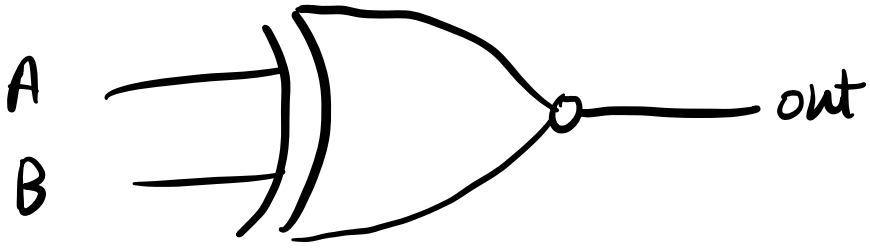


"exclusive or" operation

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

like the OR except for the last line in truth table

XNOR (NOT Exclusive OR)



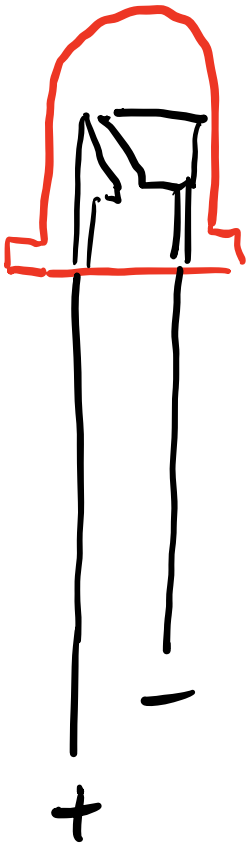
A	B	out = $\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

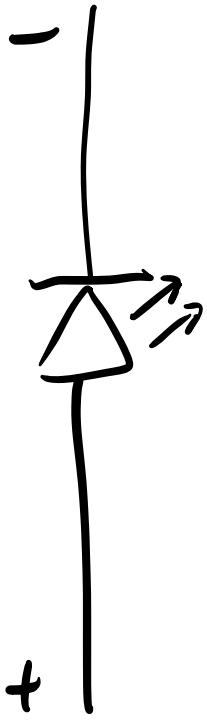
Exp. #7 Digital Basics.

Part 1. Test one of the logic gates in the lab. (NOT or NAND).

Logic gates require +5V & gnd to operate. Check data sheets on course website for pin diagrams.

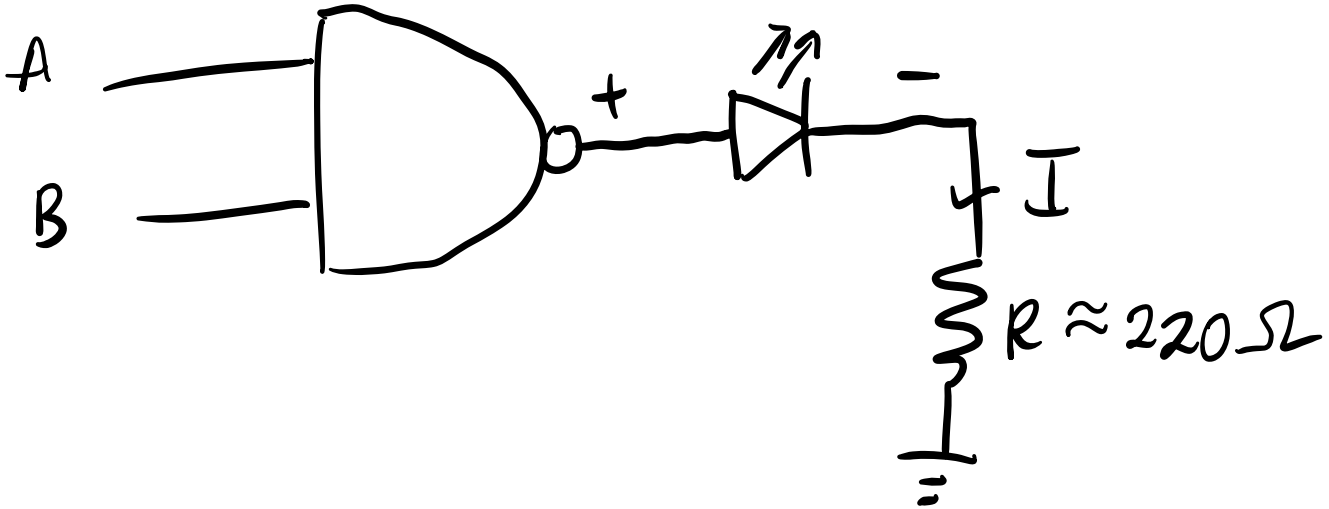
Use light-emitting diode (LED) to monitor the output of your logic gate.





when pos. terminal of LED is higher in volt. than neg. terminal, LED lights up. ($\Delta V \sim 2V$)

To test a logic gate,



The 220Ω resistor limits the current I.

Connect A & B inputs to +5V or gnd to verify expected truth table.

Part 2: Design & build an OR gate using only NAND gates (3 NANDs are required). (Only one IC is needed)

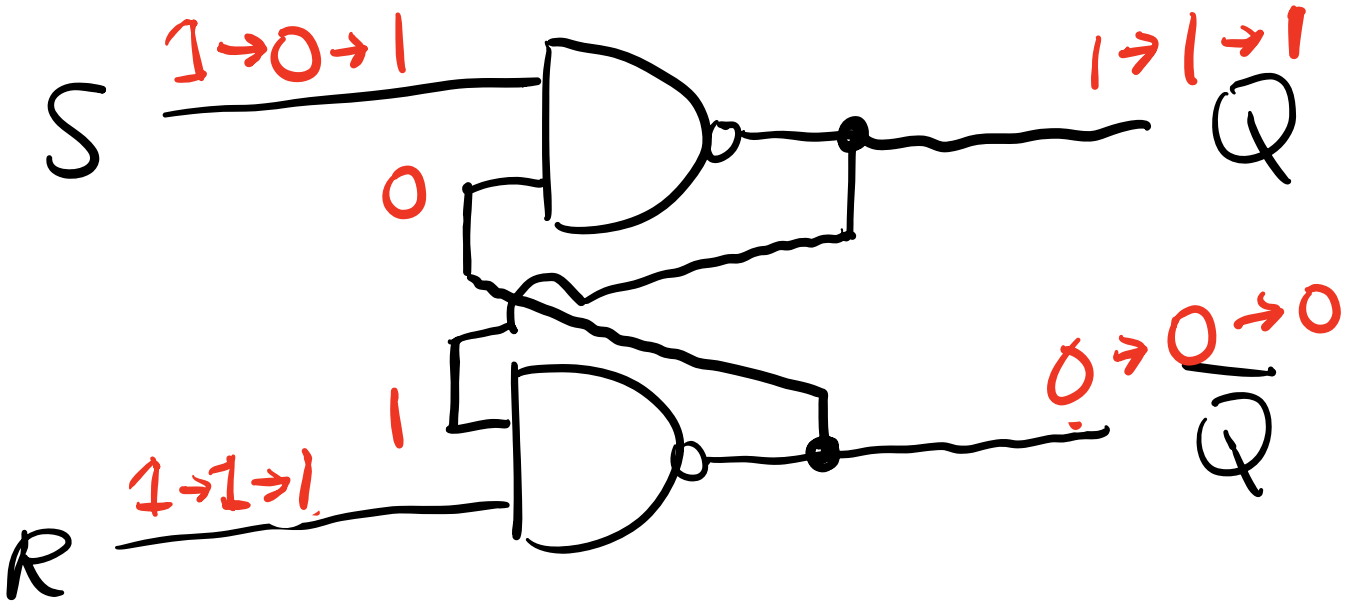
Test truth table using same method as in Part 1 (LED).

So far, all logic gate outputs depend on instantaneous states of inputs. Design a device that has some memory capability.

Flip-Flop $\Rightarrow$ R-S Flip Flop

reset set.

The R-S Flip-Flop is a two-input device (R & S) with two outputs. The state of the outputs (Q & $\overline{Q}$) tells the user which of R or S was the last to be LO. That is, the flip-flop "remembers" which of the inputs was last LO.



R-S Flip Flop.

NAND

A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

Take $(S, R) = (1, 1)$ as the default inputs.

What are the possible outputs $(Q, \bar{Q})$?

$(Q, \bar{Q}) =$ ~~$(0, 0)$~~, $(0, 1)$ ✓, $(1, 0)$ ✓, ~~$(1, 1)$~~

not possible for $(S, R) = (1, 1)$

When $(S, R) = (1, 1)$, output of flip flop has two possible stable states $\Rightarrow$ bistable.

What happens if one of S or R momentarily drops to LO?

Case 1. Initially

$S=1$	$R=1$	$Q=0$	$\overline{Q}=1$
↓	↓	↓	↓
0	1	1	0
↓	↓	↓	↓
1	1	1	0

case 2. Initially

$S=1$	$R=1$	$Q=1$	$\overline{Q}=0$
↓	↓	↓	↓
0	1	1	0
↓	↓	↓	↓
1	1	1	0

Momentarily allowing S to go LO "sets" the output state to $(Q, \overline{Q}) = (1, 0)$.

Exercise for student!

Show that, regardless of the initial state of $(Q, \bar{Q})$, allowing R to go LO temporarily "resets" the output to $(Q, \bar{Q}) = (0, 1)$.

Exp. #7 Part 3